Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

M.E DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025

First Semester

Applied Electronics

PAPT2402 - Advanced Digital System Design

Regulations - 2024

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	How many states are there in 3-bit ring counter? What are they?	L3	1	2
2.	What do you mean by the term state reduction problem?	L1	1	2
3.	Why is the pulse mode operation of asynchronous sequential circuits not very popular?	L2	2	2
4.	List any two drawbacks of asynchronous circuits.	L1	2	2
5.	Define Stuck at faults with an example.	L1	3	2
6.	Recall Path sensitization method.	L2	3	2
7.	How many data inputs, data outputs and address inputs are needed for a 1024 *4 ROM?	L3	4	2
8.	Mention the applications of PLDs.	L1	4	2
9.	List the modeling types in Verilog HDL programming.	L2	5	2
10.	Write a Verilog code for 2:1 multiplexer.	L3	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Examine an ASM chart to design a sequence detector which can detect 01101 sequences. For all other bit patterns there is no change in output.	L3	1	16
			Or			
	b	i	Inference in detail about the state assignment procedure.	L3	1	8
		ii	List the rules for state assignment. Give an example.	L3	1	8
12.	a		Summarize the design procedure for asynchronous sequential circuit with an example.	L3	2	16
			Or			
	b		A synchronous sequential circuit is described by the following excitation and output function Y=X1X2+(X1+X2)Y, Z=Y. Draw the logic diagram of the circuit and derive the transition table and output map.	L3	2	16

13.	a	Describe the procedure of designing a fault detection experiment with the help of an example.	L3	3	16
		Or			
	b	Make use of D- algorithm, explain how it is useful in the synthesize and optimize digital circuits.	L3	3	16
14.	a	Briefly explain the architecture of FPGA - Xilinx 4000 with necessary diagrams.	L3	4	16
		Or			
	b	Design a 4-bit binary counter using PAL. In the design process draw the state table, derive the logical equations and show the K map reduction. array.	L3	4	16
15.	a	With an example explain the behavioral, structural and Gate level modeling in Verilog HDL programming.	L5	5	16
		Or			
	b	Evaluate the process of Compilation and Simulation of Verilog code with an example.	L5	5	16